ABSTRACT OF THE DISCLOSURE

Apparatus embedded in a processor system comprises: an auxiliary instruction queue (IQ); and control circuits for governing the programming of registers of the auxiliary IQ with a set of instructions and for controlling insertion of the programmed instructions of the auxiliary IQ into an instruction execution stream of the processor system substantially without interrupting processing operations thereof. In another embodiment, the IQ is memory mapped to render it part of the memory space of the processor system and the control circuits govern the programming of the auxiliary IQ with a set of debug instructions accessed from a debug monitor program over the bus. In yet another embodiment, each storage register of the IQ is fabricated in the IC to survive an upset transient wherein a monitor circuit detects an onset of the upset transient and governs the control circuits to transfer data of selected registers of the processor system into the auxiliary IQ for storage during the upset transient. A method of protecting the integrated circuit (IC) processor system against an upset transient is also disclosed. In still another embodiment, the registers of the auxiliary IQ are configurable in the power-up mode to store a set of boot loader instructions which are accessible by the processor system.